WHAT IS CLAIMED IS:

1. A space vector pulse-width modulator (SVPWM) comprising:

a precalculation module which accepts Ua and Ub modulation indexes and in response thereto, outputs modified Ua and Ub information;

a sector finder having a U module which receives the modified Ua information and outputs a U sector; and a Z module which receives the U sector and the modified Ub information and outputs a Z sector;

said U sector and said Z sector being 2-phase control signals for implementing 2-phase modulation; and

for 3-phase modulation, said SVPWM further comprising:

an active vectors section which receives said modified Ua and Ub information and said U sector, and which calculates active vectors for 3-phase modulation;

a zero vector selector which receives said Z sector and calculates zero vectors for 3-phase modulation; and

a PWM counter block which receives said active vectors and zero vectors and outputs 3-phase control signals for implementing 3-phase modulation.

2. The SVPWM of claim 1, wherein said active vectors section comprises an active vectors calculation module and an assign vectors module.

3. The SVPWM of claim 1, wherein said PWM counter block has a symmetrical PWM mode.

4. The SVPWM of claim 3, wherein said PWM counter block has an asymmetrical PWM mode.

5. The SVPWM of claim 1, wherein said PWM counter block has an asymmetrical PWM mode.

6. The SVPWM of claim 1, further comprising a rescale and overmodulation module which receives duration information corresponding to said vectors and in response thereto, detects the occurrence of overmodulation.

7. The SVPWM of claim 6, wherein overmodulation is detected in response to a negative zero vector time.

8. The SVPWM of claim 7, wherein said rescale and overmodulation module responds to overmodulation by clamping the zero vector time to zero and rescaling the active vector times to fit within the PWM cycle.

9. The SVPWM of claim 8, wherein said rescaling restricts a voltage vector to stay within hexagonal boundaries on the space vector plane, while preserving voltage phase.

10. A method of implementing space vector pulse-width modulation (SVPWM) comprising the following steps:

a precalculation step which accepts Ua and Ub modulation indexes and in response thereto, outputs modified Ua and Ub information;

a sector finder step which includes the step of receiving the modified Ua information and outputting a U sector; and the step of receiving the U sector and the modified Ub information and outputting a Z sector;

wherein said U sector and said Z sector are 2-phase control signals for implementing 2-phase modulation; and

for 3-phase modulation, said SVPWM further comprising the following steps:

an active vectors calculation step which includes receiving said modified Ua and Ub information and said U sector, and calculating active vectors for 3-phase modulation;

a zero vector selection step which includes receiving said Z sector and calculating zero vectors for 3-phase modulation;

a PWM counting step which includes receiving said active vectors and zero vectors and outputting 3-phase control signals for implementing 3-phase modulation.

11. The method of claim 10, wherein said PWM counting step implements a symmetrical PWM mode.

12. The method of claim 11, wherein said PWM counting step implements an asymmetrical PWM mode.

13. The method of claim 10, wherein said PWM counting step implements an asymmetrical PWM mode.

14. The method of claim 10, further comprising an overmodulation detecting step which receives duration information corresponding to said vectors, and in response thereto, detects the occurrence of overmodulation.

15. The method of claim 14, wherein overmodulation is detected in response to a negative zero vector time.

16. The method of claim 15, wherein said method responds to overmodulation by the steps of clamping the zero vector time to zero and rescaling the active vector times to fit within the PWM cycle.

17. The method of claim 16, wherein said rescaling step restricts a voltage vector to stay within hexagonal boundaries on the space vector plane, while preserving voltage phase.